



**AFRL-RY-WP-TR-2017-0096**

**HYBRID SILICON-ON-SAPPHIRE/SCALED CMOS  
INTERFERENCE MITIGATION FRONT END BASED ON  
SIMULTANEOUS NOISE-CANCELLATION, ACTIVE-  
INTERFERENCE-CANCELLATION AND N-PATH-MIXER  
FILTERING**

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14. ABSTRACT The objective of this research was to investigate the challenges and demonstrate integrated circuit techniques for developing interference mitigation technology (IMT) enabling frequency-agile, reconfigurable filter-less receivers. Wideband noise-canceling, active-interference cancelling, and high-power handling techniques was explored. The proposed reconfigurable, wideband, agile IMT front-end enables filter-less DoD receivers. This IMT solution pushes the line of commonality in DoD receivers all the way to the antenna, greatly lowering the non-recurring engineering cost for the upgrading and maintenance of DoD receiver systems.						
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## Table of Contents

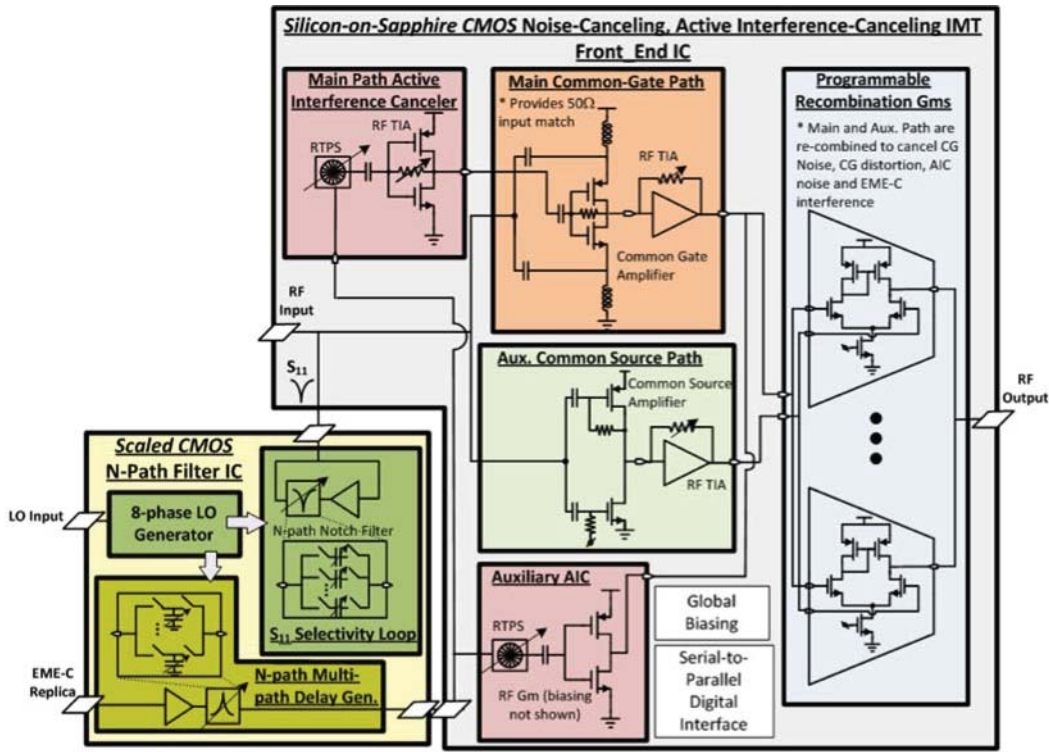
Section	Page
List of Figures .....	ii
1. INTRODUCTION .....	1
1.1 Summary of Innovative Claims.....	2
2. METHODS, ASSUMPTIONS, AND PROCEDURES.....	3
2.1 6th Order N-Path Based All Passive Filter .....	3
2.2 Magnetic-Free N-path-Filter-Based Passive Nonreciprocal Circulator .....	4
2.3 Highly-Linear Integrated Magnetic-Free Circulator-Receiver for Full-Duplex Wireless.....	6
2.4 Scalable Spatial Notch Suppression for MIMO Receiver Arrays .....	8
2.5 Ultra-Wideband Arbitrary Spatial Filtering for MIMO Receiver Arrays .....	9
3. CONCLUSIONS .....	11
4. REFERENCES .....	12
LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS .....	13

## List of Figures

Figure	Page
Figure 1: Proposed Hybrid SOS/Scaled-CMOS Noise-Cancelling, Active-Interference-Cancelling, N-Path-Mixer Filtering IMT Front End Module .....	1
Figure 2: Formation of an Arbitrary Higher-Order Filter .....	3
Figure 3: Components of Magnetic-Free Non-Reciprocal Circulator .....	5
Figure 4: Components of Highly-Linear Integrated Magnetic-Free Circulator-Receiver .....	7
Figure 5: Scalable Spatial Notch Suppression for MIMO Receiver Arrays .....	9
Figure 6: Ultra-Wideband Arbitrary Spatial Filtering for MIMO Receiver Arrays .....	10

# 1. INTRODUCTION

Typical Department of Defense (DoD) receivers employ fixed-frequency radio frequency (RF) front-end filters to protect themselves from blockers. However, fixed-frequency filters limit frequency agility and are bulky, especially when multiple switched fixed-frequency filters must be used for reconfigurable multi-standard/multi-mode operation. In order to meet DoD interference mitigation technology (IMT) needs and enable frequency-agile, reconfigurable filter-less receivers, we propose an agile, wideband (1-2GHz) two-integrated circuit (IC) IMT front-end module that can be used with existing receiver modules (RXMs) in the place of RF front-end filters (Figure 1). The proposed IMT solution pushes the line of commonality in DoD receivers all the way to the antenna, greatly lowering the non-recurring engineering (NRE) cost for the upgrading and maintenance of DoD receiver systems.



**Figure 1: Proposed Hybrid SOS/Scaled-CMOS Noise-Cancelling, Active-Interference-Cancelling, N-Path-Mixer Filtering IMT Front End Module**

The first IC is a wideband noise-cancelling, active-interference-cancelling (AIC) front end implemented in Peregrines 0.25 $\mu$ m Silicon-on-Sapphire (SOS) technology for extremely high-power signal handling. This IC uses a noise-cancelling AIC topology to perform active cancellation of multiple simultaneous +20dBm co-operative interference signals while not degrading the noise figure (NF) of the filter-less IMT-enabled receiver sub-system (RSS). The second IC uses a scaled complementary metal-oxide-semiconductor (CMOS) technology (namely 45nm SOI CMOS) to implement a frequency-agile, reconfigurable 8-path notch filter embedded in feedback to selectively reflect weaker (-20dBm) non-cooperative out-of-band interference signals, and create a highly-frequency-selective S<sub>11</sub> and filter-like transfer function profile. This IC also uses N-path bandpass filters to create large group delays to compensate for

multipath effects seen in the co-operative interference signals being cancelled by the AIC circuitry.

In short, the proposed IMT module combines the advantages of N-path filtering and active interference cancellation, as well as the advantages of scaled SOI CMOS and high-voltage silicon-on-sapphire CMOS.

## **1.1 Summary of Innovative Claims**

The proposed reconfigurable, wideband, agile IMT front-end enables filter-less DoD receivers through the following innovative concepts:

- Usage of Peregrine 0.25 $\mu$ m SOS CMOS in Conjunction with IBMs 45nm Silicon on Insulator (SOI) CMOS: The noise-cancelling AIC IMT front-end signal path is implemented in SOS CMOS to leverage the high breakdown voltage (3.5V DC) to enable cancellation of +20dBm co-operative interferers and achievement of high open-loop OOB (out-of-band) IIP3. 45nm SOI CMOS is used for the implementation of an N-path notch-filter-based S11 selectivity loop (that requires high-speed multiphase local oscillator (LO) generation) to handle weaker non-cooperative interferers.
- Wideband Noise-cancelling AIC Topology: The proposed noise-cancelling AIC topology uses a two-step AIC approach in which the noise generated by the AIC circuitry is completely cancelled. Compared to the work supported under the RF focal plane gate array (FPGA) program, SOS CMOS in conjunction with series stacking of devices is exploited to enable cancellation of multiple simultaneous +20dBm signals.
- N-path-filter-based Multipath Delay Generation: AIC has traditionally been limited by multipath effects. N-path bandpass filters are used to create high-Q filters to generate large multipath delay spreads in the replica signals used for cancellation.
- Agile, Reconfigurable N-path-notch-filter-based S11 Selectivity Loop: An N-path-notch filter is placed in active feedback loop to create a highly-selective S11 and transfer function profile, which can be reconfigured in center frequency, bandwidth (BW) and gain. New concepts that will be investigated include a stability analysis in the presence of wide variations in antenna (ANT) voltage standing wave ratio (VSWR), the usage of delay-locked loops (DLLs) rather than frequency dividers for low-power multiphase LO generation in the N-path filter, and the usage of the notch-filter-based feedback loop at other nodes, including the output, to further enhance frequency selectivity.

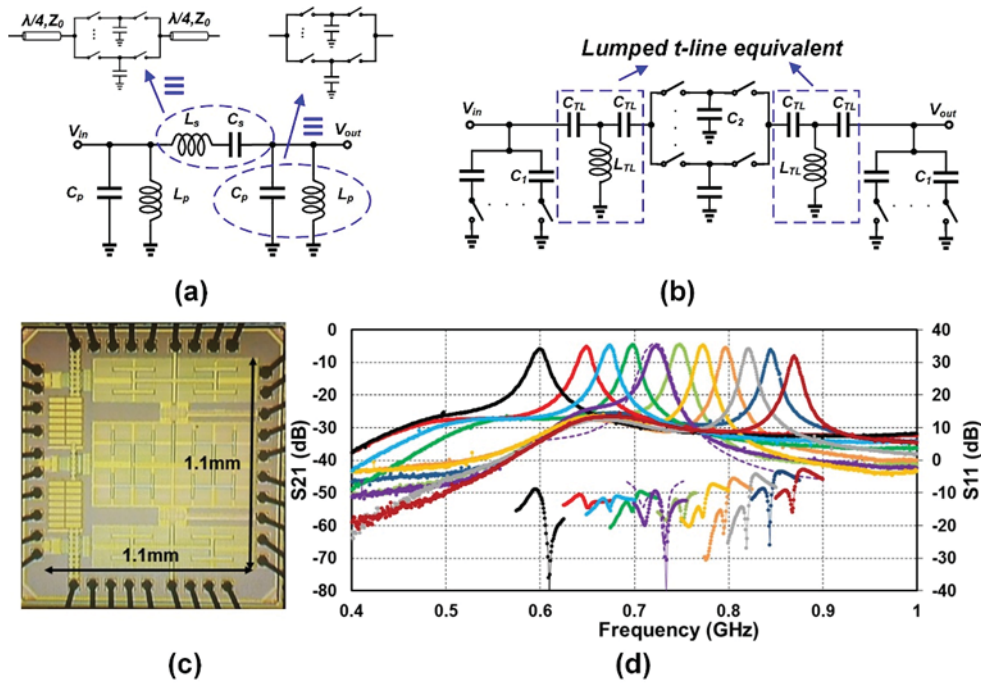
It should be mentioned that the architecture, circuit design details and innovative claims documented in this section represent the material in our original proposed work. The following sections describe our research efforts and the evolution of these ideas under the Defense Advanced Research Projects Agency (DARPA) Arrays at Commercial Timescales (ACT) program.

## 2. METHODS, ASSUMPTIONS, AND PROCEDURES

### 2.1 6th Order N-Path Based All Passive Filter

Conventional N-path filters only present second-order filter responses. While there has been research on higher-order N-path filters, these approaches use active devices which can limit the linearity and noise performance. Here, a methodology for synthesizing all-passive higher order N-path filters is proposed.

Figure 2(a) and (b) summarize the design methodology for higher-order all-passive N-path filters. Generalized filter theory provides us with a design methodology for filters of arbitrary order and filter shape based on series and shunt LC sections with known values for the L and C components. The conventional N-path filter produces a response that mimics a shunt LC section, but there is no known N-path structure that produces a series LC response. This methodology uses quarter-wave transmission lines (t-lines) to perform shunt-to-series transformation on an N-path filter, resulting in an equivalent series LC response. Combining N-path-based equivalents of shunt and series LC sections enables the formation of an arbitrary higher-order filter as shown in Figure 2.



**Figure 2: Formation of an Arbitrary Higher-Order Filter**

(a) 6th-order LC filter and shunt-LC to series-LC transformation of a two-port N-path filter using quarter-wave t-lines. (b) Proposed architecture of an all-passive 6th-order (in general, arbitrary order) N-path filter with CLC T-type quarter-wave t-line equivalents. (c) The chip microphotograph and (d) measured S21 and S11 for different clock frequencies in conjunction with reconfiguration of the CLC T-type networks. A comparison between measurement (solid) and simulations (dashed) is also shown for one frequency.

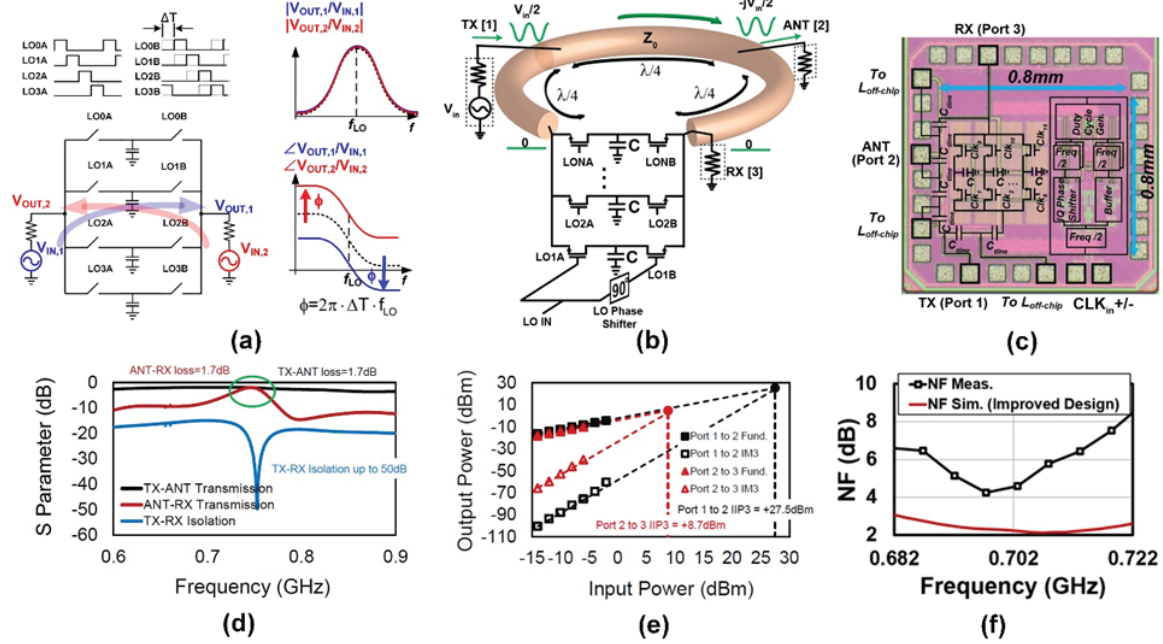
Based on this approach, a 6th order all-passive N-path filter was designed in 65nm CMOS. A prototype chip was been fabricated in 65nm CMOS (Figure 2(c)) with an active area of 1.2mm<sup>2</sup> and mounted in a QFN24 package and tested on a 4-layer printed circuit board. Each filter is implemented using 16 paths and separate clock generation has been utilized to ensure maximum symmetry in routing. The CLC t-line equivalents are implemented using switched-capacitor banks to increase the tuning range and off-chip air-core 6.9nH inductors (0806SQ from Coilcraft, typical Q=100) [1].

The implemented filter has an insertion loss of 5-6dB, a tuning range of about 35% from 640MHz to 920MHz, and filter bandwidth that ranges from 7-12MHz across the tuning range (Figure 2(d)). The filter achieves an out-of-band (OOB) rejection of 30-50 dB, input-referred in-band (IB) and OOB 1dB compression points of 0dBm and +14dBm at 300MHz offset, and input-referred IB and OOB IIP3 of +7 and +17.5dBm respectively. The clock path direct current (DC) power consumption at 700MHz is 90mW from a 1.2V supply. The proposed filter is useful for applications where sharp filtering and moderate tunability is required, such as frequency-channelized receivers, perhaps preceded by a highly-linear front-end low-noise amplifier.

## 2.2 Magnetic-Free N-path-Filter-Based Passive Nonreciprocal Circulator

Linear time-invariant (LTI) passive systems based on conventional materials are reciprocal under the Lorentz Reciprocity Theorem. A three-port, matched, reciprocal network cannot be lossless. Consequently, a three-port antenna interface with high transmit-receive (TX-RX) isolation, such as electrical balance duplexers [2], necessarily features at least 3dB loss (typically 4dB) between TX-ANT and ANT-RX. Non-reciprocal circulators avoid this fundamental 3dB loss, but rely on magnetic materials, and cannot be integrated on silicon. However, linear time-varying (LTV) systems can be non-reciprocal. In this section, we describe a fully-integrated CMOS passive non-magnetic non-reciprocal circulator based on LTV N-path filters.

Two-port N-path filters with a phase-shift between the input and output clocks have been explored as a means of adding phase shift to signals traveling through the filter [3]. Interestingly, the phase-shifts applied to signals near the switching frequency traveling in opposite directions have opposite signs (Figure 3(a)) the magnitudes of  $S_{21}$  and  $S_{12}$  are equal (and exhibit low loss for large N) but the phases of  $S_{21}$  and  $S_{12}$  are opposite in sign and equal in magnitude to the clock phase shift.



**Figure 3: Components of Magnetic-Free Non-Reciprocal Circulator**

(a) Magnetic-free non-reciprocity based on the non-reciprocal phase response of a two-port phase-shifting N-path filter. (b) 3-port circulator architecture, the RX port is placed at the right side of the N-path filter to enhance TX-ANT linearity. (c) Chip photo of the magnetic-free passive circulator. (d) Circulator S-parameter measurements. (e) Comparison of TX-ANT and ANT-RX IIP3 measurement results. (f) NF measurement results for the ANT to RX path.

To create non-reciprocal wave propagation, a  $3\lambda/4$  transmission line is wrapped around the N-path filter with +90 clock phase shift. In such a ring, signals can only propagate in one direction. In the clockwise direction, the  $-270^\circ$  phase shift of the  $3\lambda/4$  line combines with the  $-90^\circ$  shift of the N-path filter to create constructive interference. Counter-clockwise, the  $-270^\circ$  shift of the line adds with the  $+90^\circ$  shift of the N-path to create destructive interference.

A three-port circulator can be realized by introducing three ports anywhere on the transmission line, as long as they maintain a  $\lambda/4$  circumferential distance between them (Figure 3(b)). If the RX port is placed next to the N-path filter (as the case of Figure 3(b)), then for TX port excitations, the RX port, and hence one end of the N-path filter, is quiet due to the isolation of the circulator. The S-parameters of the non-reciprocal N-path filter force its two port voltages to be equal in magnitude, and consequently, its other end is quiet as well. In other words, voltage swings across the N-path filter are suppressed, resulting in high linearity to excitations at the TX port.

The circulator was designed for tunable operation around 750MHz in 65nm CMOS (Figure 3(c)). The  $3\lambda/4$  line is miniaturized using three CLC networks, with the inductors placed off-chip. 8 paths are used in the N-path filter to lower the loss. Clock phase shifting is accomplished using vector-interpolation phase shifters [4] [5].

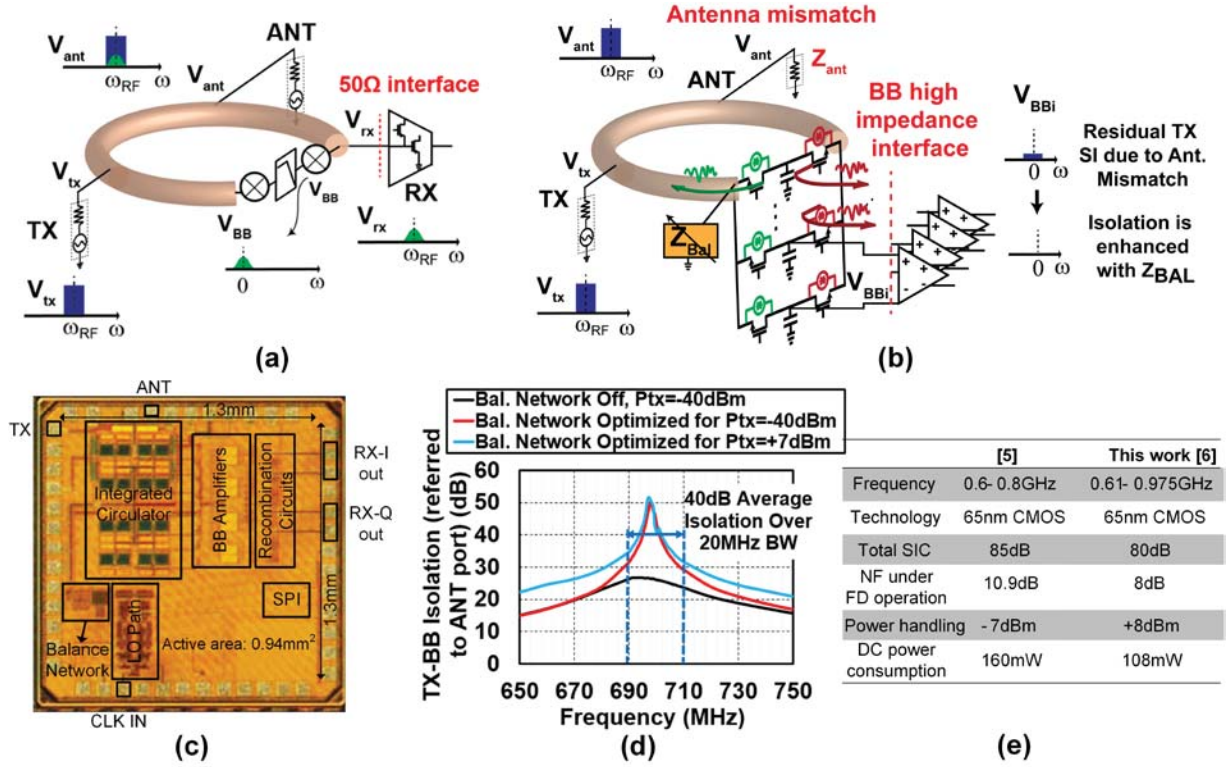
Measurements reveal 1.7dB loss in TX-ANT and ANT-RX transmission and broadband isolation better than 15dB between TX and RX (the narrowband isolation can be as high as 50dB, with a 20dB bandwidth of 32MHz) (Figure 3(d)). The measured in-band ANT-RX input third-order intercept point (IIP3) is +8.7dBm while the in-band TX-ANT IIP3 is +27.5dBm, significantly higher due to the suppression of swing across the N-path filter (Figure 3(e)). Finally, the measured ANT-RX NF is 4.3dB, degraded from the expected 2dB NF due to LO-path phase noise. Elimination of the phase shifters (not necessary as only a static +90° phase shift is desired) or using an improved phase-shifter design restores the NF to around 2dB in simulation (Figure 3(f)).

### 2.3 Highly-Linear Integrated Magnetic-Free Circulator-Receiver for Full-Duplex Wireless

In this work, we present a novel full-duplex (FD) architecture, namely a circulator-receiver [6], which (i) merges the magnetic-free passive N-path-filter-based circulator in [5] with a down-converting mixer, directly providing baseband (BB) receiver signals at its output, and (ii) incorporates an on-chip balance network into the circulator architecture to enhance the TX-RX isolation and track ANT variations. These innovations (i) lower the overall power consumption due to elimination of the RX low noise amplifier (LNA) and mixer, (ii) lower the overall NF due to the elimination of the associated sources of noise, and (iii) substantially enhance the TX power handling as the balance network greatly increases the TX-RX isolation prior to the BB amplifiers, which can also be designed with greater linearity than RF LNAs. The circulator-receiver provides 40dB of on-chip large-signal TX-RX isolation averaged over 20MHz bandwidth (2x greater bandwidth than [5]), can handle up to +8dBm of TX power (310x and 31x greater than prior shared-ANT FD RXs, [7] and [5], respectively), and exhibits 8dB NF under cancellation. In conjunction with digital self-interference cancellation (SIC) in MATLAB, 80dB overall SIC is achieved at +8dBm TX power. A FD demo shows the ability to receive a weak signal while providing 70dB total SIC to a +0dBm average-power orthogonal frequency-division multiplexing (OFDM)-like modulated TX signal.

Conventional reciprocal ANT interfaces, such as surface acoustic wave (SAW) duplexers/filters, impose a  $50\Omega$  matching requirement on the RX to obtain best filtering performance. However, a non-reciprocal circulator does not require  $50\Omega$  matching at its RX port since the reflected power will circulate, while the ANT port is still matched. Leaving the RX port open even provides 6dB of voltage gain compared to the matched case.

Interestingly, the circulator concept of [5] affords the opportunity to repurpose the N-path filter for down-conversion of incoming signals from the ANT port, eliminating the need for an additional LNA/low noise transconductance amplifier (LNTA) and mixer (Figure 4(a)). The structure becomes equivalent to a circulator merged with a zero-IF mixer-first RX, with the additional aforementioned advantage of not having to achieve  $50\Omega$  input matching in the RX. Isolation continues to be seen between the TX port and the N-path filter BB ports. An additional interesting behavior is noise circulation (Figure 4(b)) it can be shown that the noise of the RX-side switches alone contribute to RX NF while the noise of the TX-side switches circulates away. Hence, the NF of the circulator-receiver is theoretically as low as that of traditional mixer-first RXs despite the additional set of switches.



**Figure 4: Components of Highly-Linear Integrated Magnetic-Free Circulator-Receiver**  
 (a) Repurposing the N-path filter for down-conversion of incoming signals from the ANT port, eliminating the need for an additional LNA/LNTA and mixer. (b) Noise of the RX-side switches alone contribute to RX NF while the noise of the TX-side switches circulates away. (c) Circulator-receiver is designed to operate around 750MHz in 65nm CMOS. (d) Improving the average large-signal isolation to 40dB over 20MHz BW. (e) Summary of the results and comparison to prior work.

All circulators require an ANT tuner to maintain TX-RX isolation in the face of ANT variations. Inspired by the concept of the balance network in electrical-balance duplexers, we have found that incorporating a tunable impedance on the TX side of the N-path filter can maintain TX-RX isolation as the ANT impedance varies (Figure 4(b)). In essence, the tunable impedance creates a reflection that cancels out the reflected TX signal leaking to the BB nodes from the ANT port. The net result of these innovations is a merged circulator-receiver architecture for FD wireless that exhibits lower power consumption and NF than a conventional cascaded design [5] due to the elimination of the RX LNA/LNTA and mixer, and superior TX power handling than prior art due to the high TX-RX isolation prior to BB amplification (which can be designed with higher linearity than RF circuits).

The circulator-receiver is designed to operate around 750MHz in 65nm CMOS (Figure 4(c)). The  $3\lambda/4$  line is miniaturized using three CLC networks, with the inductors placed off-chip similar to before. The N-path filter BB nodes are amplified by inverter-based BB amplifiers and harmonic recombination circuitry. The on-chip balance network consists of a tunable resistive and capacitive bank. The average small-signal TX-BB isolation (referred to the ANT port) is nominally 25.8dB in Figure 4(d) over 20MHz BW. Engaging and optimizing the balance

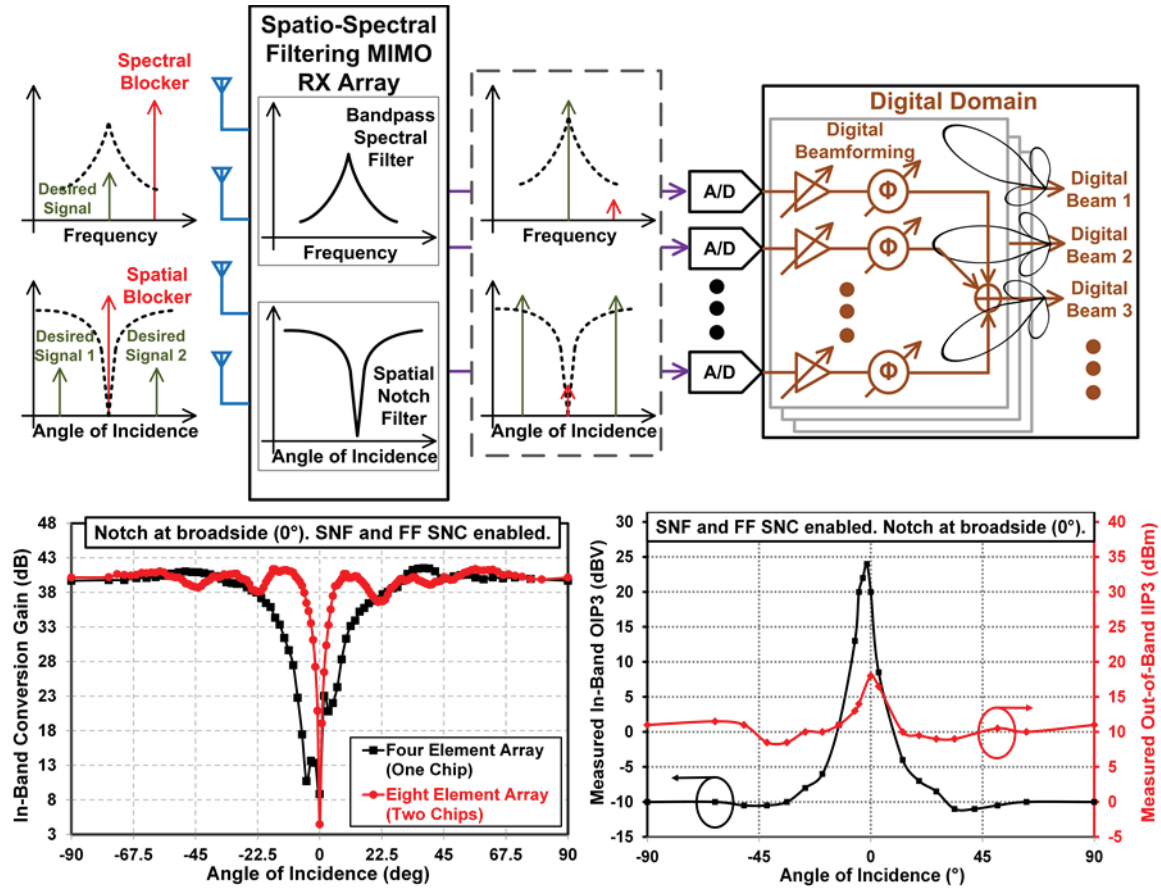
network dramatically improves the average large-signal isolation to 40dB over 20MHz BW (Figure 4(d)). At the optimized balance network setting, the NF is 8dB and the overall power consumption is 108mW. A summary of the results and comparison to prior work is shown in Figure (e).

## 2.4 Scalable Spatial Notch Suppression for MIMO Receiver Arrays

Large-scale multiple-input-multiple-output (MIMO) technology is drawing significant attention for next-generation wireless networks. Traditional MIMO receiver architectures use multiple parallel receiver front ends with digitization at every element to support flexible and powerful digital space-time array processing. Digital array calibration is also enabled by such an architecture. However, the absence of analog/RF spatial filtering in traditional digital MIMO receiver arrays results in a high dynamic-range requirement, and consequently, power-hungry analog and RF receiver front ends and analog-to-digital converters.

A scalable spatial notch suppression technique overcomes the aforementioned challenge, and is demonstrated with a 65nm CMOS 0.1-1.7GHz spatio-spectral-filtering four-element MIMO receiver array (Figure 5). The analog/RF circuits and analog-to-digital converters are protected from spatial interference early in the signal chain by the proposed spatial notch filter (SNF) and feed-forward spatial notch canceler (FF-SNC), easing their dynamic range requirement.

At in-band frequencies, spatial notch suppression can reject a spatial blocker by 32dB. The combination of spatial and spectral filtering results in more than 19dB rejection irrespective of the frequency at which the spatial blocker is located. The proposed spatial notch suppression technique improves the measured in-band output third-order intercept point (OIP3) from -10dBV to +24dBV, and the measured out-of-band IIP3 from +11dBm to +18dBm. Furthermore, turning on the spatial notch suppression leads to minimal noise figure degradation. 1.7-4.5dB noise figure is measured with spatial notch suppression turned off, whereas turning it on only mildly degrades the NF to 2.2-4.6dB. The spatial notch suppression technique is scalable across multiple ICs without the need for RF interconnections at board-level. A wireless imaging demo shows two of the implemented ICs tiled on board to form an eight-element MIMO receiver array that is able to detect a weak desired signal in the presence of an in-band 15dB-stronger spatial blocker. For additional details, the reader is directed to [8–10].



**Figure 5: Scalable Spatial Notch Suppression for MIMO Receiver Arrays**

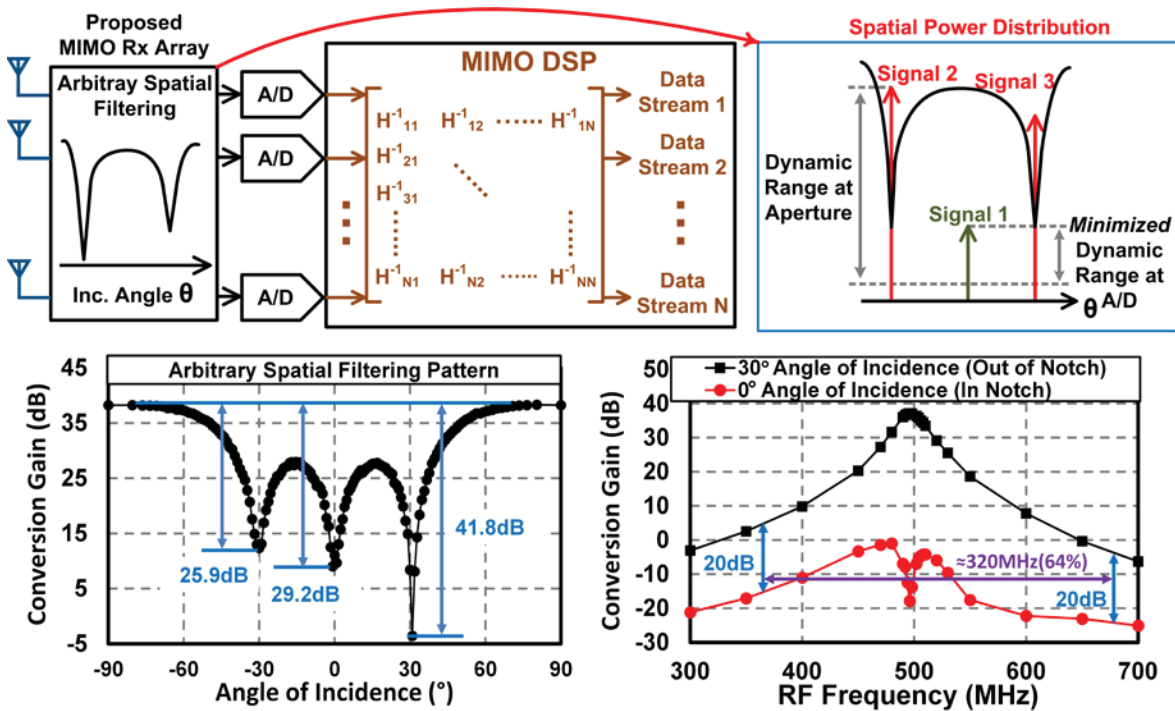
Measured spatial responses show  $>30\text{dB}$  of spatial notch suppression in the broadside direction. Two ICs can be tiled on printed circuit board (PCB) to form an 8-element MIMO receiver array that shows improved spatial selectivity. Measured in-band linearity is improved by  $34\text{dB}$  and out-of-band linearity by  $7\text{dB}$ .

## 2.5 Ultra-Wideband Arbitrary Spatial Filtering for MIMO Receiver Arrays

The aforementioned spatial notch suppression technique can reject a single spatial blocker, but it can be insufficient in the presence of multiple strong spatial signals, or in a multi-path scattering scenario. In addition, the existing spatial notch suppression technique operates in the voltage domain, which leads to limited linearity and low suppression bandwidth.

Instead of a single spatial notch, a more flexible and robust solution, namely an arbitrary spatial filtering technique, is proposed. According to the actual power distribution in the spatial domain, this technique allows the adaptive synthesis of such a spatial response that provides high conversion gains to weak spatial signals, and low gains to the strong ones. As all the spatial signals pass through the receiver array and reach analog-to-digital converters, they all have the same power level, therefore only demanding the minimum dynamic range from the data converters. Such an equalization operation in the spatial domain is carried out with current-mode circuits that avoid large voltage swings for strong spatial signals, ensuring superior linearity. The current-mode operation also helps expand spatial suppression bandwidth.

A 0.1-to-3.1GHz 4-element MIMO receiver array is implemented to validate the arbitrary spatial filtering (ASF) technique. A single spatial notch can be synthesized to an arbitrary direction, consistently achieving more than 50dB of suppression. An arbitrary number of notches, independently steered to arbitrary directions, can be synthesized, with all the notch depths freely adjusted. The implemented arbitrary spatial filtering functionality improves measured linearity by 33dB at in-band frequencies, and 17dB at out-of-band frequency. Inside the notch direction, an ultra-wide 320MHz spatial suppression bandwidth (20dB) is measured at 500MHz LO frequency, corresponding to a 64% bandwidth. With the arbitrary spatial filtering on, measured single-element-equivalent double-sideband noise figure ranges from 3.4 to 5.8dB across all operating frequencies. A wireless demo shows that the arbitrary spatial filtering allows the reception of a weak modulated signal in the presence of two 11-dB stronger spatial signals with limited analog-to-digital conversion dynamic range. For additional details, the reader is directed to [11].



**Figure 6: Ultra-Wideband Arbitrary Spatial Filtering for MIMO Receiver Arrays**

*Measured arbitrary spatial response features three spatial notches steered to arbitrary directions with adjustable notch depths. At 500MHz LO frequency, frequency response inside the notch direction shows >20dB spatial suppression in addition to spectral filtering over 320MHz, or equivalently 64% bandwidth.*

### 3. CONCLUSIONS

This proposed reconfigurable, wideband, agile IMT front-end enables filter-less DoD receivers through the following innovative concepts:

- Usage of peregrine 0.25 $\mu$ m SOS CMOS in conjunction with IBMs 45nm SOI CMOS
- Wideband noise-cancelling AIC topology
- N-path-filter-based multipath delay generation
- Agile, reconfigurable N-path-notch-filter-based S11 selectivity loop

The IMT solution described in this report pushes the line of commonality in DoD receivers all the way to the antenna, greatly lowering the NRE cost for the upgrading and maintenance of DoD receiver systems.

## 4. REFERENCES

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## LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
ACT	Arrays at Commercial Timescales
AIC	active-interference-cancelling
ANT	antenna
ASF	arbitrary spatial filtering
BB	baseband
BW	bandwidth
CMOS	complementary metal-oxide-semiconductor
DARPA	Defense Advanced Research Projects Agency
DC	direct current
DLL	delay-locked loop
DoD	Department of Defense
FD	full-duplex
FF-SNC	feed-forward spatial notch canceler
FPGA	focal plane gate array
IB	in-band
IC	integrated circuit
IIP3	input third-order intercept point
IMT	Interference Mitigation Technology
LNA	low noise amplifier
LNTA	low noise transconductance amplifier
LO	local oscillator
LTI	linear time-invariant
LTV	linear time-varying
MIMO	multiple-input-multiple-output
NF	noise figure
NRE	non-recurring engineering
OFDM	orthogonal frequency-division multiplexing
OIP3	output third-order intercept point
OOB	out-of-band
PCB	printed circuit board
RF	radio frequency
RSS	receiver sub-system
RXM	receiver module
SAW	surface acoustic wave
SIC	self-interference cancellation
SNF	spatial notch filter
SOI	silicon on insulator
SOS	silicon-on-sapphire
TX-RX	transmitter-receiver
VSWR	voltage standing wave ratio